

Energy-aware MPC co-design for DC-DC converters

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Abstract—In this paper, we propose an integrated controller design methodology for the implementation of an energy-aware explicit model predictive control (MPC) algorithms, illustrating the method on a DC-DC converter model. The power consumption of control algorithms is becoming increasingly important for low-power embedded systems, especially where complex digital control techniques, like MPC, are used. For DC-DC converters, digital control provides better regulation, but also higher energy consumption compared to standard analog methods. To overcome the limitation in energy efficiency, instead of addressing the problem by implementing sub-optimal MPC schemes, the closed-loop performance and the control algorithm power consumption are minimized in a joint cost function, allowing us to keep the controller power efficiency closer to an analog approach while maintaining closed-loop optimality. A case study for an implementation in reconfigurable hardware shows how a designer can optimally trade closed-loop performance with hardware implementation performance.

I. INTRODUCTION

DC-DC converters are employed for a wide range of solutions, spanning from low to high power electronics. A common request is the need for voltage regulation of their inputs/outputs over a wide range of operating conditions, while maximizing power conversion efficiency (thus minimizing power losses). Traditionally, voltage control has been implemented in an analog fashion. However, in the last few years, analog controllers have been gradually replaced by digital ones [1], [2].

Such a shift from analog to digital has been more predominant in high power applications, where the power losses introduced by a digital controller are negligible compared to the total losses of the converter. This explains why analog solutions are still prevalent for low power applications. For these applications, the overall cost of the converter, in terms of its construction and its power consumption, is a major driving factor. If one also considers the requirements of physical size and weight, it becomes clear why analog control is still the preferred choice. Analog control, however, brings many limitations. A new analog integrated circuit has to be designed for each specific application and external discrete electronic components (such as capacitors and resistors) introduce additional uncertainties due to their tolerances [3].

To overcome these limitations, in the last few years there has been significant interest in moving to digital control techniques. Starting from basic controller formulations (PID) [4], we have seen an evolution going all the way to on-line

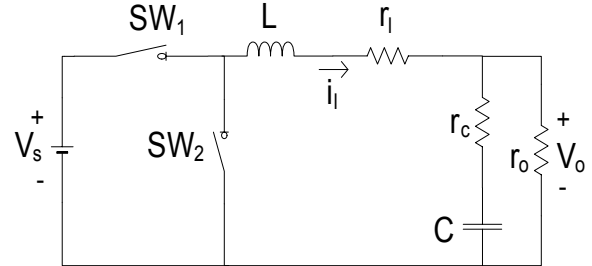


Fig. 1. Step-down synchronous DC-DC converter.

optimization-based techniques like model predictive control (MPC) [5]–[8]. The main drawback with MPC is that the increase in algorithm complexity requires more computation. The result is an increase in power losses compared to an analog alternative [9]. So far, the solutions proposed to overcome this issue are based on approximation and are therefore sub-optimal [10].

To address this efficiency problem, we propose a co-design methodology where an explicit MPC controller is designed together with its implementation on the target embedded computing platform. This approach departs from the standard practice where control engineers design a controller assuming that its hardware implementation is a separate decoupled problem. It will be shown that a high degree of coupling is indeed present. For instance, the choice of the data representation affects both the closed-loop performance and hardware specifications like power consumption, chip size, etc. The smaller the number of bits used for the data representation, the smaller the chip size and its power consumption, but the higher the round-off errors and therefore the less accurate the control actions become.

We proceed by posing a multi-objective optimization problem to optimally trade controller design, in terms of power consumption, with regulation performance. We show how the proposed co-design approach can be successfully applied to a digitally controlled DC-DC converter. The case study shows that levels of power conversion efficiency close to those of analog controllers can be obtained while retaining all the good features of an MPC scheme without sacrificing closed-loop optimality.

II. STEP-DOWN DC-DC CONVERTERS

A synchronous step-down or buck DC-DC converter [3] is a switching electronic circuit (Fig. 1) used to transform an input voltage V_s into a lower output desired voltage V_o . It is based on two switches SW_1 and SW_2 , cascaded by a second order LC low-pass filter and by an output ohmic load r_o . The capacitor C and the inductor L have been considered respectively with their internal ESR (r_c) and resistance (r_l).

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To stabilize the output voltage against load, input voltage and component variations, feedback control is necessary. For every switching period T_{sw} the output voltage and the current that flows in the inductor i_l are read and used to manipulate the opening and closing time of the two switches. When SW_1 is closed, SW_2 is opened and the input power is transferred to the output through the inductor. This is for a time equal to $d(t) \cdot T_{sw}$, where $d(t) \in [0, 1]$ is the duty cycle. For the remaining time $(1 - d(t)) \cdot T_{sw}$ of the switching period, the switches' status are swapped providing a path for the inductor current i_l . This behavior is repeated during each switching period.

The above system operation leads to its description through a switched continuous-time model based on a set of linear and time-invariant mathematical models, one for each operating condition. Let us define the state vector as $x(t) := [i_l(t) V_o(t)]^T$, then the system behaves as

$$\dot{x}(t) = A_c x(t) + b_c, \quad (1)$$

when SW_1 is closed, and as

$$\dot{x}(t) = A_c x(t), \quad (2)$$

when SW_2 is closed. The output voltage is given by

$$V_o(t) := c_c^T x(t). \quad (3)$$

Matrices A_c , b_c and c_c are given by

$$A_c := \begin{bmatrix} \frac{1}{C} \frac{r_o}{r_o + r_c} \left(1 - C r_c \frac{r_l}{L}\right) & -\frac{1}{C} \frac{1}{r_o + r_c} \left(1 + C r_c \frac{r_o}{L}\right) \\ \frac{1}{r_o + r_c} \frac{C}{L} & 0 \end{bmatrix}, \quad b_c := \begin{bmatrix} \frac{1}{r_o + r_c} \frac{C}{L} \\ 0 \end{bmatrix}, \quad c_c := [0 \ 1]^T. \quad (4)$$

For control purposes, this hybrid model may not be suitable. A large number of DC-DC converter modeling techniques have been proposed in the last few years [11]–[13] and a widely-used approach is the state-space averaging method [14]. This produces an average continuous-time model that merges the laws of the hybrid model and that uses the duty cycle $d(t)$ as an input variable. The result is a nonlinear mathematical model that describes the system behavior accurately if the switching period T_{sw} is much smaller than the time constant of the LC low-pass filter. The controller design can be carried out by linearizing the model around an operating point.

According to the averaging method, the state-space average model of the step-down converter (1)-(2) is described by

$$\begin{aligned} \dot{x}(t) &= A_c x(t) + b_c \cdot d(t), \\ V_o(t) &= c_c^T x(t). \end{aligned} \quad (5)$$

This is a linear system where the states can be directly measured, the input is the duty cycle $d(t)$ and the output is the output voltage $V_o(t)$. Furthermore, there are constraints resulting from the converter topology. The duty cycle has to be between 0 and 1, and, for safety reasons, be less than its saturation value i_{lmax} . Hence, a controller design that can handle constraints efficiently is necessary.

III. OPTIMAL CONTROLLER AND HARDWARE CO-DESIGN

Our objective is to design a constrained controller for the DC-DC converter that is not only optimal in a closed-loop sense, but also in an energy sense, i.e. it minimizes the power dissipated by its own implementation. This is relevant in a DC-DC converter where its objective is to convert power, ideally without absorbing any itself. The most important industrial performance index used to evaluate the quality of a DC-DC converter is its power conversion efficiency η defined as

$$\eta := \frac{P_o}{P_o + P_{loss}}, \quad (6)$$

where P_o is the output power and P_{loss} is the total power loss of the converter electronic components (mainly the inductor and switches) and the control circuitry.

Since reducing power consumption is a main concern for efficiency, it is reasonable to assume that the control algorithm is implemented in a low-power embedded computing platform like field-programmable gate arrays (FPGAs) or application-specific integrated circuits (ASICs). Among other features, FPGAs and ASICs offer a great degree of design flexibility (including custom data representation, parallel computation and pipelining [15]) that can be used as implementation optimization parameters.

Consider the discrete-time feedback control law

$$u_k := \kappa(x_k), \quad (7)$$

where $\kappa : \mathbb{R}^n \rightarrow \mathbb{R}$ is designed to stabilize and guarantee some performance for the discretized DC-DC converter model in (5):

$$x_{k+1} = A x_k + b u_k, \quad (8)$$

where, for a constant input (zero-order-hold), $A := e^{A_c T_s}$, $b := \left[\int_0^{T_s} e^{A_c \tau} d\tau \right] b_c$ and T_s is the sampling time (which also corresponds to the converter switching period T_{sw}).

Let $J_{cl}(\kappa, T_s, \Gamma)$ be a closed-loop performance measure of the controller κ in feedback (via a sampler with period T_s and a zero-order-hold) with the system in (5). The parameter Γ represents, generally, the data representation accuracy and arithmetic precision. The closed-loop performance is a function of Γ because the round-off errors introduced by a finite arithmetic unit are effectively perturbations on the control signal. In the linear case, $J_{cl}(\kappa, T_s, \Gamma)$, with Γ being an infinite precision arithmetic system, could be an H_∞ norm of the closed-loop plant or, for LQR, the trace of the solution of the Riccati equation (the cost expectation subject to random initial conditions). No analytical result exists for our case and such a cost will have to be obtained via other means (we will use simulations in Section IV-B).

Let $J_{pw}(\kappa, T_s, \Gamma, \theta)$ be the hardware implementation performance measure defined in terms of electrical power dissipated by the hardware platform. The variable θ is a set of hardware-specific parameters (such as the processor's clock frequency) and architecture-related parameters (such as the number of algorithm threads that can be executed in parallel). Note that the sampling time T_s and the data representation

TABLE I
BUCK CONVERTER SETUP

Parameter	Value	Parameter	Value
V_s [V]	6	r_l [mΩ]	15.5
V_o [V]	1	i_{lmax} [A]	4
r_o [mΩ]	500	C [μF]	68
L [μH]	1.5	r_c [mΩ]	1.5

TABLE II
MULTI-OBJECTIVE OPTIMIZATION PROBLEM VARIABLES' RANGE

Variable	Range
T_s [μs]	2.5 – 3.33
Γ [bits]	1 – 52
f_{clk} [MHz]	10 – 300
p [number of parallel threads]	1 – 1000
l [latency in clock cycles]	1 – 10

Γ could be included in θ but they are considered separately because they are also in the domain of J_{cl} .

Minimizing both the closed-loop and the energy cost functions is a multi-objective optimisation problem that can be posed as

$$\min_{\kappa, T_s, \Gamma, \theta} [J_{cl}(\kappa, T_s, \Gamma), J_{pw}(\kappa, T_s, \Gamma, \theta)] \quad (9a)$$

$$s.t. : r(\kappa, T_s, \Gamma, \theta) \leq r_{MAX}, \quad (9b)$$

where $r(\cdot, \cdot, \cdot, \cdot)$ is a vector-valued function that represents the platform resources utilized such as memory, silicon area and clock frequency. The vector r_{MAX} contains the maximum available resources for a particular platform. Budget parameters such as hardware market value and development costs could also be included. As a note of interest, although it might seem obvious to also constrain the computational latency to be smaller than T_s , this is not necessary for customizable hardware since parallelization and pipelining allow computational delays to be longer than the sampling time [16]. The solution to the multi-objective problem (9) can be posed in terms of Pareto optimality and efficiency (for a single point solution) or compromise solutions (see [17] for a tutorial).

The cost functions J_{cl} and J_{pw} are coupled by parameters such as the controller structure, the sampling time and the data representation. For instance, fast sampling times lead to a better closed-loop performance (faster reaction to disturbance rejection). However, higher power consumption is also associated with faster sampling, mainly for two reasons: i) a higher computing power is needed to guarantee real-time execution; ii) a more accurate data representation is needed to overcome rounding errors, more likely to happen at high sampling frequencies [18], [19].

Such complex trade-offs, normally addressed sub-optimally, if considered at the design stage can greatly improve the performance of a DC-DC converter application where hardware and control algorithms are pushed to the limits of their capabilities.

IV. CASE STUDY SETUP

For benchmarking purposes, a low-power (2 Watt) Buck converter setup has been designed with Texas Instrument

SwitcherPro software [20]. Table I shows its principal electrical characteristics. According to the control objectives, the electrical characteristics of the selected converters and the target embedded computing platform, the variables of the multi-objective optimization problem (9) are now defined for this specific case.

The controller κ is an explicit MPC lookup-table [21] (the problem formulation is given in Section IV-A) that we want to implement in a low cost Spartan-6 Xilinx XC6SLX45 FPGA [22]. During the last few years, many FPGA implementations of explicit MPC have been proposed [23]–[25]. Within these solutions we have chosen to implement the one [25] where the point location algorithm [21], the most computationally demanding part, is based on a multi-way tree. This approach is preferred because its flexibility gives us the freedom to easily tune many hardware-specific parameters. The parameter Γ is here an integer that defines the fraction length, in terms of number of bits, of a fixed-point number system, thus it represents the precision of the arithmetic components (by design, we use enough bits for the integer part so that overflow does not occur). The hardware-specific parameters are defined as $\theta = (f_{clk}, p, l)$, where: f_{clk} is the circuit clock frequency; p is the number of *children* for each node of the multi-way tree [25] i.e. the parallelism in terms of the number of algorithm threads (children's membership checks) that can be executed simultaneously; l is the latency of mathematical operators in the FPGA circuit. These are generally the main tuning parameters for FPGA circuit design [26].

The optimization is performed over a set of discrete variables. Some variable spaces, such as the one for Γ , are finite and discrete by nature. Other variable spaces, such as the one for T_s , are taken within a finite range and considered at discrete step intervals. The set of all variable and their ranges are given in Table II. The ranges have been chosen with engineering judgment in order to explore the solution space effectively and with sufficient precision. The multi-objective optimization problem in (9) is solved over this set of variables via an exhaustive exploration of the solution space. This problem is solved off-line and an exhaustive enumeration is possible in a limited amount of time.

Definitions for the controller design, closed-loop cost $J_{cl}(\kappa, T_s, \Gamma)$, power consumption cost $J_{pw}(\kappa, T_s, \Gamma, \theta)$ and constraint function $r(\kappa, T_s, \Gamma, \theta)$ are given in the following sections.

A. Design of controller κ

Consider the continuous-time, finite horizon LQ problem defined by the cost function

$$J_c := x(T)' P x(T) + \int_0^T \begin{bmatrix} x(t) \\ u(t) \end{bmatrix}' \begin{bmatrix} Q_c & 0 \\ 0 & R_c \end{bmatrix} \begin{bmatrix} x(t) \\ u(t) \end{bmatrix} dt, \quad (10)$$

where $Q_c = I$, $R_c = 1$, P is the solution of the discrete-time Riccati equation and $T = 40\mu s$ is the prediction horizon. These values are given to define a controller for an ideal closed-loop performance of the continuous-time model in (5). We assume that the input is constant between sampling

instants (zero-order hold). The equivalent sampled-data cost function is therefore

$$J_{T_s} := x'_N P x_N + \sum_{k=0}^{N-1} \begin{bmatrix} x_k \\ u_k \end{bmatrix}' \begin{bmatrix} Q & M \\ M' & R \end{bmatrix} \begin{bmatrix} x_k \\ u_k \end{bmatrix}, \quad (11)$$

where N is the number of samples for the predicted horizon, defined as $N := \lceil T/T_s \rceil$, $\lceil \cdot \rceil$ is the ceiling function and expressions for Q , R , M and P can be found in [27]. We assume full state feedback. Let $x_k := x$ be the state measured at sample instant k and x_j , where $j \in \mathbb{N}_0$, be the predicted state at $k+j$ for the given initial state x and an input sequence $\mathbf{u} := (u_0, u_1, \dots, u_{N-1})$. The MPC problem is defined as

$$\min_{\mathbf{u}} \quad x'_N P x_N + \sum_{j=0}^{N-1} \begin{bmatrix} x_j \\ u_j \end{bmatrix}' \begin{bmatrix} Q & M \\ M' & R \end{bmatrix} \begin{bmatrix} x_j \\ u_j \end{bmatrix}, \quad (12a)$$

$$\text{s.t.} \quad x_{j+1} = A x_j + B u_j, \quad x_0 = x, \quad (12b)$$

$$[0, 0]^T \leq x_{j+1} \leq [i_{lmax}, V_s]^T, \quad (12c)$$

$$0 \leq u_j \leq 1, \quad (12d)$$

$$j = 0, 1, \dots, N-1. \quad (12e)$$

The solution of this problem can be computed explicitly [21] using the Multi Parametric Toolbox (MPT) [28]. The result is a feedback controller κ defined as a piecewise affine (PWA) function over tens of polytopic regions in two dimensions. Note that MPT does not readily allow for the inclusion of the mixed input-state term M . This problem can be resolved by applying a change of variables to eliminate M [29, Lemma 5] and by modifying the input-state constraints accordingly.

B. Closed-loop cost function J_{cl}

Because of the lack of analytical results for the computation of the closed-loop cost of constrained systems with controller round-off errors, a closed-loop cost is measured by averaging the costs of 10^3 simulations of the controlled plant evolution from a set of random and uniformly distributed initial condition to steady state. Hence, we define it as

$$J_{cl}(\kappa, T_s, \Gamma) := \sum_{j=0}^{N_{cl}-1} \begin{bmatrix} x_j \\ \langle u_j \rangle_{\Gamma} \end{bmatrix}' \begin{bmatrix} Q & M \\ M' & R \end{bmatrix} \begin{bmatrix} x_j \\ \langle u_j \rangle_{\Gamma} \end{bmatrix}, \quad (13)$$

where $N_{cl} := \lceil T_{cl}/T_s \rceil$, u_k is given in (7) and $\langle \cdot \rangle_{\Gamma}$ is the rounded-off value for a fixed-point number representation using Γ bits for the number's fractional part and enough bits for the integer part in order to avoid overflow. Time T_{cl} is chosen long enough so that $x_j \approx 0$ and $\langle u_j \rangle_{\Gamma} \approx 0$ for all $j \geq N_{cl}$ and all feasible initial conditions.

C. Power consumption cost J_{pw} and resource constraints

The cost J_{pw} is the dynamic power consumption for a given set of parameters (Γ, f_{clk}, p, l) of the circuit implementation of controller κ designed for the discretized plant model with sampling time T_s . Analytical results of FPGA power consumption are not generally available. In order to have accurate and realistic data, a model of the hardware power consumption, resource utilization and computational delay has been built empirically by designing and building a large number of circuits using the available Xilinx ISE

TABLE III
SELECTED POINTS FROM THE PARETO FRONTIER

Variable	#A	#B	#C
J_{cl}^r	1.551	1.019	1
J_{pw} [mW]	0.483	1	160
T_s [μ s]	3.33	3.33	2.5
Γ [bits]	3	5	47
f_{clk} [MHz]	300	300	300
p [number of parallel threads]	5	5	2
l [latency in clock cycles]	1	2	6

software development tool [22], and accurately simulating the circuit behavior with the Mentor Graphics Modelsim software [30]. For a wide range of operating conditions the circuit's resource allocation and delays were measured and the power consumption estimated. The results were then interpolated polynomially using MATLAB's curve fitting function `polyfit`. The result was a 2-degree polynomial model, since the relationship between Γ and the power consumption of arithmetic operators follows approximately a square law. For $(f_{clk}, p, \frac{1}{l})$ these relationships are approximately linear [31]. Hence, we have that

$$J_{pw} \propto \Gamma^2, f_{clk}, p, \frac{1}{l}, \quad (14)$$

which can be explained as follows. An increase in the number of bits (Γ), the clock frequency (f_{clk}) and the number of algorithm threads to be executed simultaneously (p) results in an increase in computing hardware resources (silicon) and therefore higher power consumption. Increasing Γ , for instance, means utilizing more hardware resources to store data and to perform computations. On the other hand, power is inversely proportional to the latency of the FPGA multiplier operator's (l), since an increase in latency reduces the amount of short circuit glitches [32]. The sampling time T_s also affects the power. At this stage, we assume that the computational delay must be shorter than the sampling time (although not strictly necessary [16]). Hence, the smaller T_s , the faster the control action has to be computed and therefore the more power is required.

The resource constraint function in (9b) has again been obtained using the Xilinx ISE software development tool, which allowed us to build a map of resources utilization for given $(\kappa, T_s, \Gamma, f_{clk}, p, l)$. The resources we constrain are the available number of DSPs (digital signal processors), FFs (flip-flops), LUTs (look-up tables) and clock frequency (although possibly unusual, we treat the maximum clock speed as a resource). The vector r_{MAX} contains the maximum available number of such resources in the selected FPGA. These data were obtained from the manufacturer data sheets [22].

V. CASE STUDY RESULTS

A. Pareto optimality analysis

The solution of the multi-objective optimization problem (9) is a Pareto frontier curve. Let us define a normalized closed-loop cost function J_{cl}^r as the ratio between $J_{cl}(\kappa, T_s, \Gamma_{fixed})$, measured with a fixed-point arithmetic controller implementation, and $J_{cl}(\kappa, T_s, \Gamma_{double})$, measured

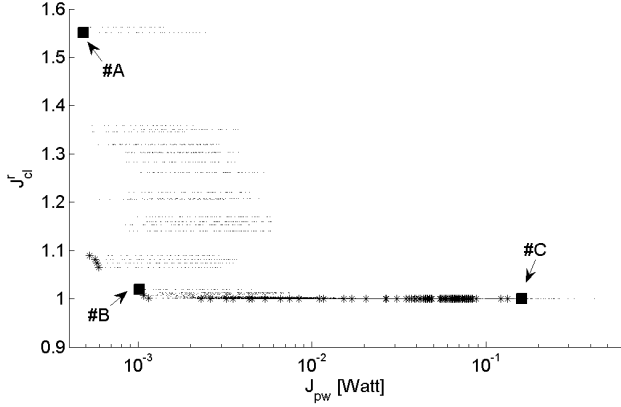


Fig. 2. Results of the exhaustive exploration (dots) of the state space for the multi-objective optimization problem (9). The Pareto frontier (stars) expresses the optimal design trade-offs between the closed-loop and power cost function. Among the solutions over the Pareto frontier, three relevant configurations (squares) have been selected, and details are given in Table III.

with double precision floating-point arithmetic. Figure 2 shows the Pareto frontier, thus the design trade-off between J_{cl}^r and the FPGA power consumption J_{pw} . High control performance (J_{cl}^r closer to 1) is achievable only by consuming a fair amount of power. A smaller power consumption can be obtained at the expense of closed-loop performance. Thus, the selection of a suitable design among the ones along the Pareto frontier can be accomplished according to high-level project specifications.

In Table III, three possible design choices, extracted from Figure 2, are highlighted: design #A favors power consumption, design #C control performance and design #B is an in-between trade-off.

Recall that the closed-loop cost J_{cl} , as defined in Section IV-B, is a function of the sampling period T_s and the data representation Γ . Figure 3 shows the variation of J_{cl}^r as the number of bits Γ increases for three fixed sampling periods. As Γ increases, J_{cl}^r tends to 1, i.e. $J_{cl}(\kappa, T_s, \Gamma_{fixed})$ approaches $J_{cl}(\kappa, T_s, \Gamma_{double})$. This is expected, since higher precision arithmetic introduces smaller round-off errors. It is interesting to notice that a low number of bits (as low as 7) seems to be sufficient for an acceptable closed-loop performance. Hence, from the hardware resources viewpoint, the commonly used double precision floating-point arithmetic would be wasteful in this case.

Figure 4 shows the relationship between the power consumption of the implemented circuit and Γ for a fixed set of sampling frequencies. As Γ increases, more hardware resources are requested for storing data and performing computations, and consequently J_{pw} increases. Furthermore, for the same Γ , J_{pw} also increases as the sampling period decreases. This happens because the parameters f_{clk} and p are changing. In fact, in order to meet tighter time constraints, either or both the clock frequency f_{clk} and the amount of parallel threads p for region location need to increase. Higher power consumption is the result of a higher clock frequency and a larger silicon area needed for parallel search.

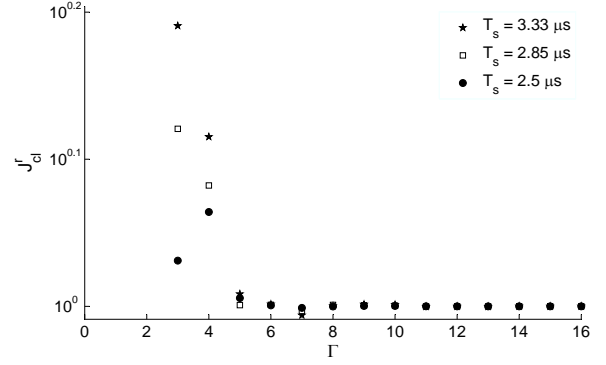


Fig. 3. Closed-loop cost as a function of the data representation Γ and the sampling frequency.

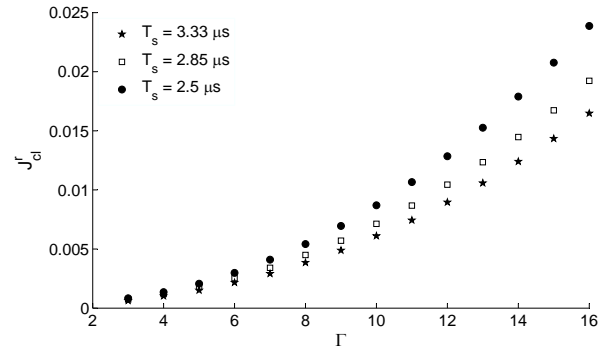


Fig. 4. Power cost as a function of data representation Γ and the control sampling frequency.

B. Efficiency comparison

The converter efficiency has been computed as in (6). Because the DC-DC converter is digitally controlled, the plant outputs have to be read, converted to digital form by means of an ADC¹ and used by the controller (the FPGA) to compute the control action. As an example, Table IV reports the efficiency and an estimation of the principal losses associated with the DC-DC converter for a selection of designs #A, #B, #C (from the Pareto frontier of Figure 2). The ADC loss is provided by the manufacturer, while the inductor, switches and FPGA losses have been computed as the sum their dynamic and static power. The static FPGA power is assumed to be constant and this is provided by the manufacturer. Its dynamic power depends on the design parameters and it corresponds to J_{pw} in Table III. It should be noted how moving from a high power consumption design #C to a low power one #A, allows one to trade-off the overall converter efficiency against performance. In some cases the efficiency (or the power consumption) can be improved without significantly degrading the closed-loop performance (e.g. when moving from design #C to design #B).

We conclude by pointing out that the proposed tuning methodology allows us to design a digitally controlled low-

¹Analog to Digital Converter (ADC). A 400kSPS AD7701 [33] ADC was considered.

TABLE IV
DC-DC CONVERTER EFFICIENCY AND MAIN LOSSES

Component	#A	#B	#C
η_d [%]	86.56	86.54	80.57
L [mW]	62	62	62
SW_1, SW_2 [mW]	188	188	200
ADC [mW]	37	37	37
FPGA [mW]	23.5	24	183

power DC-DC converters with an efficiency closer to an analog-controlled one, as we show next. In order to make a comparison between the two approaches, starting from the converter topology presented in the test case, an analog controller has been applied, i.e. the ADC and the FPGA have been replaced by a suitable commercial analog controller.² This resulted in a power conversion efficiency of 88.38%, which is comparable to the efficiency of the digital energy-aware designs in Table IV.

VI. CONCLUSIONS

We have proposed a control and hardware co-design approach for DC-DC converters. Hardware implementation issues were considered at the design stage so that the closed-loop performance of the MPC scheme and the power conversion efficiency, in terms of algorithm energy consumption, where optimized simultaneously. This method allows the designer to optimally trade the closed-loop and hardware implementation performance. The multi-objective optimization problem was solved via simulation and exhaustive search. Future work could integrate this method with an analytical approach for MPC design that is robust against round-off errors (i.e. the round-off errors are considered a priori).

VII. ACKNOWLEDGMENTS

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²The results are for a TPS54218 [20].

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